IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1(Original). A method of optimizing packet length for wireless transmissions, comprising the steps of:

selecting a trial packet length value;

determining a packet success rate for the trial packet length value;

evaluating a rate measure value for the trial packet length value, based upon the packet success rate for the trial packet length value;

adjusting the trial packet length value responsive to a difference in the rate measure value for the trial packet length value from a prior rate measure value for a prior trial packet length value; and

repeating the selecting, determining, evaluating, and adjusting steps until a convergence criterion is reached.

2(Original). The method of claim 1, further comprising:

selecting a learning constant value;

wherein the adjusting step comprises:

multiplying the difference in rate measure values by the learning constant value; and

adjusting the trial packet value by an amount corresponding to the result of the multiplying step.

3(Original). The method of claim 1, wherein the step of determining a packet success rate comprises:

applying the trial packet length value to a packet success rate function.

4(Original). The method of claim 1, wherein the step of determining a packet success rate comprises:

measuring an actual packet success rate for a plurality of transmitted packets having the trial packet length value.

5(Original). The method of claim 1, wherein the rate measure value corresponds to a product of the packet success rate and a ratio of the payload portion of each packet to an overall packet length including interpacket spacing.

6(Original). The method of claim 1, further comprising:

estimating an expected packet error rate based upon a signal-to-noise ratio of a channel;

evaluating an actual packet error rate from the actual transmissions of packets over the channel; and

comparing the actual packet error rate to the expected packet error rate;

wherein the selecting, determining, evaluating, adjusting, and repeating steps are performed responsive to the result of the comparing step.

7(Original). The method of claim 6, wherein the selecting, determining, evaluating, adjusting, and repeating steps are performed responsive to the comparing step determining that the actual packet error rate exceeds the expected packet error rate by at least a selected threshold amount.

8(Original). A wireless local area network adapter, comprising:

an interface, for coupling the adapter to a host computer;

radio circuitry, for transmitting and receiving signals over an antenna, the transmitted signals being in the form of packets including a payload portion and a preamble portion, with successive packets being transmitted with a selected interpacket spacing therebetween;

signal processing circuitry, coupled between the interface and the radio circuitry, for modulating signals to be transmitted by the radio circuitry, and for demodulating signals received by the radio circuitry; and

programmable logic, for optimizing the length of the payload portion of the packets, programmed to optimize the length of the payload portion of the packets by executing a sequence of operations comprising:

selecting a trial packet length value;

determining a packet success rate for the trial packet length value;

evaluating a rate measure value for the trial packet length value, based upon the packet success rate for the trial packet length value;

adjusting the trial packet length value responsive to a difference in the rate measure value for the trial packet length value from a prior rate measure value for a prior trial packet length value;

repeating the selecting, determining, evaluating, and adjusting steps until a convergence criterion is reached; and

then setting the length of the payload portion of each of the packets according to the trial packet length value upon the convergence criterion being reached.

9(Original). The adapter of claim 8, wherein the sequence of operations performed by the programmable logic further comprises:

selecting a learning constant value;

wherein the adjusting operation comprises the steps of:

multiplying the difference in rate measure values by the learning constant value; and

adjusting the trial packet value by an amount corresponding to the result of the multiplying step.

10(Original). The adapter of claim 8, wherein the operation of determining a packet success rate comprises the step of:

applying the trial packet length value to a packet success rate function.

11(Original). The adapter of claim 8, wherein the operation of determining a packet success rate comprises the step of:

measuring an actual packet success rate for a plurality of transmitted packets having the trial packet length value.

12(Original). The adapter of claim 8, wherein the rate measure value corresponds to a product of the packet success rate and a ratio of the payload portion of each packet to an overall packet length including interpacket spacing.

13(Original). The adapter of claim 8, wherein the sequence of operations performed by the programmable logic further comprises:

estimating an expected packet error rate based upon a signal-to-noise ratio of a channel;

evaluating an actual packet error rate from the actual transmissions of packets over the channel; and

comparing the actual packet error rate to the expected packet error rate;

wherein the sequence of the selecting, determining, evaluating, adjusting, and repeating operations is executed responsive to the result of the comparing step.

14(Original). The adapter of claim 13, wherein the sequence of the selecting, determining, evaluating, adjusting, and repeating operations is executed responsive to the comparing operation determining that the actual packet error rate exceeds the expected packet error rate by at least a selected threshold amount.

15(Original). The adapter of claim 8, wherein the signal processing circuitry comprises:

a baseband processor, for modulating and demodulating signals to be transmitted and received, respectively; and

medium access control circuitry, coupled to the interface, for processing signals to be modulated and received demodulating signals.

16(Original). The adapter of claim 15, wherein the programmable logic comprises an embedded central processing unit;

and wherein the embedded central processing unit, the baseband processor, and the medium access control circuitry are integrated into a single integrated circuit.

17 – 18. Canceled.